1) Fixed instruction length is a feature of one of the following architecture.
   a) CISC
   b) **RISC**
   c) X86
   d) None of the above

2) Which of the following register in ARM7 is used to point to the location of currently executing instruction in a program?
   a) R1
   b) R5
   c) **R15**
   d) R8

3) Evaluate the following statements and select the appropriate answer given from the choices below.
   I.   Von Neumann Architecture shares common memory for Data and Instructions
   II.   Harvard Architecture has separate physical memories for Data and Instructions
   a) Only I is true
   b) Only II is true
   c) **Both I and II are true**
   d) None of them is true

4) If the Most Significant Byte (MSB) is stored first while ordering byte values for storing data in memory, it is called as
   a) **Big-endian**
   b) Little-endian
   c) Big- and Little-endian
   d) None of them

5) How do **Direct Addressing Mode** instructions compare with respect to the **Indirect Addressing Mode** instructions?
   a)   **Faster**
   b)   Slower
   c)   No difference
   d)   None of the above

6) Which of the following processors belong to Reduced Instruction Set Computers (RISC) family?

   a) ARM
   b) AVR
   c) MIPS
   d) **All of the above**

7) Stack is a form of
   a) **Last In First Out (LIFO)**
   b) First In First Out (FIFO)
   c) Both a and b
   d) None of the above

8) A CPU wrote 'register content' into the memory in a Big-endian mode. When the same content is read back from the memory into a register, the CPU reads it in Little-endian mode.
   a) **The new content in the register will be different from what was written.**
   b) The content will be the same.
   c) The content may be same or different.
   d) Endianness need not be the same while reading and writing the contents into/from the memory.

9) Which of the following statements are true
   I.   In Little endian mode it is easier to determine a sign of the number
   II. Little endian mode is easier for addition and multiplication of multi-precision numbers
   III. Big endian mode is easier to divide two numbers
   IV. Big endian mode is easier to compare two numbers

   a) I & II are true
   b) III & IV are true
   c) I & III are true and II and IV are false
   d) **I & II are false and III and IV are true**

10) Consider a four bit ALU which does four bit arithmetic. When the following four bit numbers are added, what is the status of NZCV flags?
     1101
    + 1011
    a) NZCV = 0111
    b) NZCV = 1000
    c) NZCV = 1001
    d) **NZCV = 1010**

11) In the ARM Nomenclature **ARMxTDMI,** D and M stand for
    a) **Debug and Fast Multiplier units are present**
    b) Division and Multiplier units are present
    c) Debugger and Multiplier units are not present
    d) Division and Multiplier units are not present

12) The MCLK speed can be reduced to allow access to _____.
   a) Faster peripherals
   b) Slower peripherals
   c) CPU
   d) All of the above

13) A bus cycle requestthat transfers to or from an address which is unrelated to the address used in the preceding cycle is called a _____.
   a) Sequential Cycle
   b) Internal Cycle
   c) Non-Sequential Cycle
   d) Coprocessor Register Transfer Cycle

14) Evaluate the following statements
   I.   R13 is traditionally used as the stack pointer and stores the head of the stack in the current processor mode
   II. R14 is the link register where the core puts the return address on executing a subroutine
   III. R15 is the program counter and contains the address of the next instruction to be fetched
   a) All the options are true
   b) I and II are true
   c) II and III are true
   d) I and III are true

15) How many bits are required to specify the Register operands in anARM7 instruction?
   a) 32 bits
   b) 16 bits
   c) 4 bits
   d) 2 bits

16) When the processor is executing simple data processing instructions, the pipeline enables one instruction to be completed every clock cycle, this is also called as _____
   a) Throughput
   b) Latency
   c) Execution
   d) None of the above

17) If an instruction takes 3 cycles for execution, then how many cycles are needed for executing4 instructions of the same type in a sequence using a 3-stage pipeline? Assume that there are no interrupts or exceptions while executing them.
   a) 12 cycles
   b) 6 cycles
   c) 9 cycles
   d) 4 cycles

18) Which of the following statements are true with respect to pipelining.
   I.   Pipelining is an implementation technique whereby multiple instructions are overlapped in execution. It is not visible to the programmer
   II.   Each step is called a pipe stage or pipe segment
   III. Pipeline machine cycle is the time required to move an instruction one step down the pipeline
   a) **All are true**
   b) I and III are true
   c) II and III are true
   d) None of them are true

19) Control signals can be categorized by the pipeline stage that uses them. Which one of the following signal could be used in the Execution stage of an instruction?
   a) MemRead
   b) RegWrite
   c) **ALUop**
   d) PCsrc

20) When the number of stages in a pipeline increases from 3 to 5, then the _____.
   a) Throughput reduces
   b) Latency reduces
   c) **Throughput and latency increases**
   d) Throughput increases and latency reduces

21) State whether the following statement is either true or false. Reset vector is the location of the first instruction executed by the processor when power is applied. This instruction branches to the initialization code.
   a) **True**
   b) False

22) An instruction that is used to move data from an ARM Register to a Status Register (CPSR or SPSR) is called _____.
   a) MRC
   b) MRS
   c) **MSR**
   d) MCS

23) Instruction used to Test equality of two 32-bit values in ARM7 is called _____.
   a) **TEQ**
   b) TST
   c) EOR
   d) None of the above

24) Instruction used to multiply R5 contents by R4 and to store the result into R6 is called
   _____.
   a) MUL R6, R5, LSL #2
   b) **MUL R6, R5, R4**
   c) MUL R6, R5, LSR #2
   d) None of the above

25) Which among the following data processing instructions does not use the barrel shifter?
   a) **ADD R2, R5, R4**
   b) MOV R5, R4, LSL #2
   c) MOV r5, R4, LSR #2
   d) MOV r5, R4, ROR #2

26) If the initial register contents of R0, R1 and R2were
   R0= 0x00000000
   R1= 0x02040608
   R2= 0x10305070
   Assume R0 is the result register, after one of the operations below was performed on R1 and R2, which has been modified to R0 = 0x12345678
   What was the operation performed on the contents of R2 and R1?
   a) AND
   b) **ORR**
   c) BIC
   d) MUL

27) R1 = 0b1111
   R2 = 0b0101
   BIC R0, R1, R2
      a) **R0 = 0b1010**
      b) R0 = 0b1111
      c) R0 = 0b0101
      d) R0 = 0b1100

28) Status of Z flag after the execution of CMP instruction given below, when
   R0 = 12; R9 = 12; is
   CMP R0, R9
      a) **Z = 1**
      b) Z = 0
      c) Same as previous value
      d) None of the above

29) What are the contents of R1 and R2after
MVNR1 R2 are executed, assume R2 is 0x01010101
a) i) R2 = 0x01010101 ii) R1 = 0x01010101
b) i) R2 = 0x01010101 ii) R1 = 0x10101010
c) i) R2 = 0x10101010 ii) R1 = 0x01011101
d) i) R2 = 0x01100110 ii) R1 = 0x01010101

30) Equivalent of Rd = NOT(Rm) this operation is performed by which instruction
a) MVN
b) NEG
c) EOR
d) TST

31) Which of the following instruction ignores Operand1
a) MOV
b) MUL
c) ADD
d) SUB

32) The Logical Instructions are: ORR, EOR, TEQ, AND, TST, BIC, MOV, MVN
Why is the V flag unaffected by the logical data processing instructions?
a) Since V flag and C flag are always the same after any logical operations
b) Because it will delay the execution of logical operations
c) V flag is relevant only when an Arithmetic operation is performed
d) None of the above

33) A data processing instruction where PC(R15)is written into takes the following cycles
for execution:
a) 1S
b) 1S+I
c) 2S+1N
d) 2S+1N+1I

34) Using only two instructions, add a 64-bit integer contained in R2 and R3 to another
64-bit integer contained in R0 and R1, and place the result in R4 and R5.
a) ADD r4, r0, r2 ; ADC r5, r1, r3 ;
b) ADDS r4, r0, r2 ; ADCS r5, r1, r3 ;
c) ADD r4, r0, r2 ; ADD r5, r1, r3 ;
d) ADD r4, r0, r2 ; ADCS r5, r1, r3 ;

35) State whether the following statement is either true or false. We can represent any
number in more than one normalized notation.
a) True
b) **False**

36) In a 32- bit IEEE 754 notation, biased value of exponent value ranges
from_____.
a) **-126 to 127**
b) 0 to 127
c) -126 to 0
d) None of the above

37) State whether the following statement is either true or false. Mantissa and exponent
will improve the range and precision respectively.
a) True
b) **False**

38) Exponent and fraction values for a denormalized number are
a) 0, 0
b) $0 < E < Max$, Any bit pattern
c) All 1's, Any bit pattern
d) **0, Any non-zero bit pattern**

39) Minimum possible denormalized number representation is possible with single
precision IEEE 754 format is
a) 2^{-126}
b) 2^{-127}
c) **2^{-149}**
d) 2^{-128}

40) Vector processor architecture falls under the following computer architecture
a) SISD
b) MIMD
c) **SIMD**
d) MISD

41) Vector Floating Point (VFP) architecture is power efficient because of reduction in
_____ and _____.
a) **Instruction bandwidth and Data hazard checking**
b) Instruction bandwidth and pipelining
c) Data Hazard checking and pipelining
d) All of the above

42) Vector Floating Point (VFP) architecture provides _____floating point
architectures.
a) Single precision
b) Double precision
c) **Both a and b**
d) None of the above

43) If Vector Floating Point (VPF) has to handle 8-single precision numbers, VPF architecture must have _____ processing elements that work in parallel.
   a) 8
   b) 16
   c) 24
   d) 1

44) MRC, MCR are the _____.
   a) Co-processor register transfer instructions
   b) Thumb instructions
   c) Both a and b
   d) Shift instructions

45) The fastest data access is provided using _____.
   a) Caches
   b) DRAM's
   c) SRAM's
   d) Registers

46) The memory which is used to store acopy of data or instructions stored in larger memories, inside the CPU is called _____.
   a) **Level 1 cache**
   b) MMU
   c) Registers
   d) TLB

47) In the memory hierarchy, as the speed of memory accessincreases the memory size_____.
   a) Increases
   b) **Decreases**
   c) Both
   d) None of the above

48) Size of L1 cache compared to that of L2 cache in a system is _____.
   a) Higher
   b) Lower
   c) Same
   d) None of the above

49) Coherence means
   a) Multiple copies of different data are not available at each level of hierarchy.
   b) **Multiple copies of same data are available at each level of hierarchy.**
   c) Single copy of data is available at only one level of hierarchy.
   d) Multiple copies of different data are available at only one level of hierarchy.

50) State whether the following statement is either true or false. In direct mapping, the presence of the block in memory is checked with the help of block field.
   a) True
   b) False

51. If the access time of a cache is 1nS, and the access time of a main memory is 15nS, assuming that the Cache hit rate is 0.9 and the total number of accesses are 100; then the average access times of the access with cache and without cache will be
   _____ and _____.
   a) 250 nS and 1500 nS
   b) 250mS and 150 nS
   c) 25 nS and 1500nS
   d) 250mS and 1500mS

52. Cache design elements are
a) Block size
b) Cache size
c) Mapping functions
d) All of the above

53. The method of mapping the consecutive memory blocks to consecutive cache blocks is called _____.
   a) Set associative
   b) Associative
   c) Direct
   d) Indirect

54. State whether the following statement is either true or false. The set associative map technique combines the benefits of the direct and associative mapping techniques.
   a) **True**
   b) False

55. The memory blocks in Main Memory are mapped on to the cache blocks with the help of _____.
   a) Hash functions
   b) Vectors
   c) Mapping functions
   d) None of the above

56. The average time required to reach a storage location in memory and obtain its contents is called_____.
   a) Latency time
   b) Access time
   c) Turnaround time
   d) Response time

57. Memory unit accessed by its content is called_____.
    a) Read only memory
    b) Programmable Memory
    c) Virtual Memory
    d) Associative Memory

58. "Write Back" cache write policy is more efficient in a system where ____.
    a) Number of writes are more than reads
    b) Number of reads are more than writes
    c) Does not depend on the number of reads and writes
    d) None of the above

59. Cache memory acts between_____.
    a) CPU and Main Memory
    b) CPU and FPU
    c) MMU and Hard Disk
    d) None of these

60. The idea of cache memory exploits the following property of programs _____.
    a) Principle of locality
    b) on the heuristic 90-10 rule
    c) on the fact that references generally tend to be farther
    d) all of the above

61. Write Through technique is used in one of the following to write the data back.
    a) Virtual memory
    b) Main memory
    c) Auxiliary memory
    d) Cache memory

62. The amount of time required to read a block of data from a disk into memory
    is composed of seek time, rotational latency, and transfer time. Rotational latency
    refers to _____.
    a) the time it takes for the platter to make a full rotation
    b) the time it takes for the read-write head to move into position over the
       appropriate track
    c) the time it takes for the platter to rotate the correct sector under the head
    d) none of the above

63. Which of the following is the reason that the Least Recently Used (LRU) algorithm is usually not used as a page replacement algorithm?
    a) Other practical schemes such as MIN do a better job
    b) LRU requires knowledge of the future to work correctly
    c) LRU is too inefficient to implement in practice
    d) The Clock algorithm always outperforms LRU

64. State whether the following statement is either true or false. Increasing the block size of cache memory is likely to increase performance primarily because programs exhibit spatial locality.
    a) True
    b) False

65. State whether the following statement is either true or false. Address of any data in cache memory always refers to the address of the data in Main Memory and not the address within the cache.
    a) True
    b) False

66. In an Operating System, each process has its own _____.
    a) address space and global variables
    b) open files
    c) pending alarms, signals and signal handlers
    d) all of the above

67. What is inter-process communication?
    a) Communication within the process
    b) Communication between two processes
    c) Communication between two threads of same process
    d) None of the above

68. A scheduling algorithm can use either _____ priority or _____ priority.
    a) static, still
    b) static, dynamic
    c) live, dead
    d) None of the above

69. The priority of a process will _____ if the scheduler assigns it a static priority.
    a) change
    b) remain unchanged
    c) depend on the operating system
    d) None of the above

70. State whether the following statement is either true or false. In a system with Unified cache, access to data in the cache may impact program execution as well.
   a) **True**
   b) False

71. The L1 cache is typically split into _____ and _____ cache for the pipelined system
   a) Instruction, Data
   b) Instruction, Instruction
   c) Data, Data
   d) All of the above

72. State whether the following statement is either true or false. In a multilevel system cache system, the L2 cache may contain data that is not found in L1 cache.
   a. True
   b. False

73. Memory management technique in which the OSstores and retrieves data from secondary storage for use in main memory is called _____.
   a) Fragmentation
   b) Paging
   c) Mapping
   d) None of the above

74. Run time mapping from virtual to physical address is done by _____
   a) Memory Management Unit
   b) CPU
   c) PCI
   d) None of the above

75. Operating System maintains the page table for _____.
   a) Each data element
   b) Each instruction
   c) Each address
   d) Each process

76. _____ is the concept in which a process memory is copied into the main memory from the secondary memory according to the requirement.
   a) Paging
   b) Demand paging
   c) Segmentation
   d) Swapping

77. A process is **thrashing** if _____.
   a) **it is spending more time paging management than executing**
   b) it is spending less time paging than executing
   c) page fault occurs very infrequently
   d) swapping could not take place

78. A Page Table contains information on the page including _____.
   a) Base address of each page in physical memory
   b) Page read/write permissions
   c) Page was written into or not
   d) **All of the above**

79. A virtual memory system uses 'First In First Out' (FIFO) page replacement policy and allocates a fixed number of frames to a process. Consider the following statements:
   P: Increasing the number of page frames allocated to a process sometimes increases the page fault rate
   Q: Some programs do not exhibit locality of reference
   which of the following is TRUE?
   a) Both P and Q are true, and Q is the reason for P
   b) Both P and Q are true, but Q is not the reason for P
   c) **P is false but Q is true**
   d) Both P and Q are false

80. When a page is selected for replacement, and its modify bit is set :
   a) the page is clean
   b) **the page has been modified since it was read in from the disk**
   c) **the page is dirty**
   d) a and b

81. When a global variable may be modified by an exception handler, it should be declared as:
   a) Constant
   b) Static
   c) Dynamic
   d) **Volatile**

82. State whether the following statement is either true or false. Interrupt signal can stop the execution of an assembly instruction in the middle while it is being executed.
   a) **False**
   b) True

83. State whether the following statement is either true or false. Full technical specifications of the target hardware, memory map of the target system may not be available during SW development in most of the cases.
   a. **True**
   b. False

84. When semi-hosting is executed, the debug agent _____.
   a. **Suspends program execution**
   b. Continues program execution
   c. Both a and b
   d. None of the above

85. ELF means _____
   a. External Library Format
   b. **Executable and Linkable Format**
   c. Exclusive Loadable Format
   d. None of the above

86. Which of the following is not one of the source files of a linker to form an executable?
   a. .obj
   b. **.lef**
   c. .so
   d. .lib

87. Choose the correct order for default memory map
   a. RW->RO->ZI
   b. ZI->RO->RW
   c. **RO->RW->ZI**
   d. RO->ZI->RW

88. State whether the following statement is either true or false. A high performance bus can be connected to a low performance bus without bridge.
   a. True
   b. **False**

89. When a transfer is required the APB bus moves into the _____.
   a. hold state
   b. **setup state**
   c. Rising state
   d. None

90. The multi-layer architecture acts as a crossbar switch between_____ ina AMBA 3 AHB
   a. **Master and slave**
   b. Master and master
   c. Slave and slave
   d. None of the above

91. Which of the following may not be on the APB bus
   a. USART
   b. **RAM**
   c. Keypad
   d. Timer module

92. The main advantage of multiple bus organization over the single bus is _____.
   a. **Reduction in the number of cycles for execution**
   b. Increase in size of the register
   c. Better connectivity
   d. None of the above

93. By default DMA is not a _____.
   a. **Master**
   b. Slave
   c. Clock
   d. All of the above

94. Frequency of sampling is called _____.
   a. **Sampling rate**
   b. Quantization
   c. Modulation
   d. All of the above

95. A band limited signal can be reconstructed exactly if it is sampled at a rate atleast
   a. Maximum frequency
   b. **Twice the maximum frequency**
   c. Thrice the maximum frequency
   d. All of the above

96. Main advantage of the PWM is that _____.
   a. Power loss in the switching devices is very high
   b. **Power loss in the switching devices is very low**
   c. No power loss in switching devices
   d. None of the above

97. I^{2}C master features:
   a. Programmable I^{2}C address detection
   b. Clock generation
   c. Stop bit detection
   d. All of the above

98. The two I2C signals are _____ and _____.
   a. Serial data, serial clock
   b. Serial select, serial access
   c. Serial address, parallel data
   d. Parallel address, Parallel clock

99. Serial Peripheral Interface bus allows _____.
   a. Half/full
   b. Synchronous
   c. Serial communication with external devices
   d. All of the above

100. Thumb-2 technology enhances the 16 bit Thumb instruction set with
   a. Intermixing of 32 bits and 16 bits instructions
   b. Only 32 bits instructions
   c. Only 16 bits instructions
   d. None of the above